Route design power

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| Tool Version : Vivado v.2021.1 (win64) Build 3247384 Thu Jun 10 19:36:33 MDT 2021

| Date : Wed Apr 10 16:12:17 2024

| Host : DESKTOP-4LK3EFH running 64-bit major release (build 9200)

| Command : report\_power -file UART\_power\_routed.rpt -pb UART\_power\_summary\_routed.pb -rpx UART\_power\_routed.rpx

| Design : UART

| Device : xc7z020clg400-1

| Design State : routed

| Grade : commercial

| Process : typical

| Characterization : Production

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Power Report

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1. Summary

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| Total On-Chip Power (W) | 0.184 |

| Design Power Budget (W) | Unspecified\* |

| Power Budget Margin (W) | NA |

| Dynamic (W) | 0.077 |

| Device Static (W) | 0.107 |

| Effective TJA (C/W) | 11.5 |

| Max Ambient (C) | 82.9 |

| Junction Temperature (C) | 27.1 |

| Confidence Level | Low |

| Setting File | --- |

| Simulation Activity File | --- |

| Design Nets Matched | NA |

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\* Specify Design Power Budget using, set\_operating\_conditions -design\_power\_budget <value in Watts>

1.1 On-Chip Components

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| On-Chip | Power (W) | Used | Available | Utilization (%) |

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| Clocks | 0.023 | 3 | --- | --- |

| Slice Logic | 0.016 | 26875 | --- | --- |

| LUT as Logic | 0.014 | 6442 | 53200 | 12.11 |

| F7/F8 Muxes | 0.002 | 3264 | 53200 | 6.14 |

| Register | <0.001 | 16716 | 106400 | 15.71 |

| CARRY4 | <0.001 | 4 | 13300 | 0.03 |

| Others | 0.000 | 7 | --- | --- |

| Signals | 0.026 | 20195 | --- | --- |

| I/O | 0.012 | 20 | 125 | 16.00 |

| Static Power | 0.107 | | | |

| Total | 0.184 | | | |

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1.2 Power Supply Summary

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| Source | Voltage (V) | Total (A) | Dynamic (A) | Static (A) | Powerup (A) | Budget (A) | Margin (A) |

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| Vccint | 1.000 | 0.073 | 0.065 | 0.008 | NA | Unspecified | NA |

| Vccaux | 1.800 | 0.011 | 0.000 | 0.010 | NA | Unspecified | NA |

| Vcco33 | 3.300 | 0.004 | 0.003 | 0.001 | NA | Unspecified | NA |

| Vcco25 | 2.500 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vcco18 | 1.800 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vcco15 | 1.500 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vcco135 | 1.350 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vcco12 | 1.200 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vccaux\_io | 1.800 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vccbram | 1.000 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| MGTAVcc | 1.000 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| MGTAVtt | 1.200 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| MGTVccaux | 1.800 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vccpint | 1.000 | 0.017 | 0.000 | 0.017 | NA | Unspecified | NA |

| Vccpaux | 1.800 | 0.010 | 0.000 | 0.010 | NA | Unspecified | NA |

| Vccpll | 1.800 | 0.003 | 0.000 | 0.003 | NA | Unspecified | NA |

| Vcco\_ddr | 1.500 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vcco\_mio0 | 1.800 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vcco\_mio1 | 1.800 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vccadc | 1.800 | 0.020 | 0.000 | 0.020 | NA | Unspecified | NA |

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1.3 Confidence Level

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| User Input Data | Confidence | Details | Action |

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| Design implementation state | High | Design is routed | |

| Clock nodes activity | High | User specified more than 95% of clocks | |

| I/O nodes activity | Low | More than 75% of inputs are missing user specification | Provide missing input activity with simulation results or by editing the "By Resource Type -> I/Os" view |

| Internal nodes activity | Medium | User specified less than 25% of internal nodes | Provide missing internal nodes activity with simulation results or by editing the "By Resource Type" views |

| Device models | High | Device models are Production | |

| | | | |

| Overall confidence level | Low | | |

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2. Settings

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2.1 Environment

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| Ambient Temp (C) | 25.0 |

| ThetaJA (C/W) | 11.5 |

| Airflow (LFM) | 250 |

| Heat Sink | none |

| ThetaSA (C/W) | 0.0 |

| Board Selection | medium (10"x10") |

| # of Board Layers | 8to11 (8 to 11 Layers) |

| Board Temperature (C) | 25.0 |

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2.2 Clock Constraints

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| Clock | Domain | Constraint (ns) |

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| sys\_clk\_pin | clk | 10.0 |

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3. Detailed Reports

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3.1 By Hierarchy

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| Name | Power (W) |

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| UART | 0.077 |

| fifo\_rx | 0.042 |

| fifo\_tx | 0.015 |

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